AK

| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,759 | KU ET AL. | |
| | Examiner | Art Unit | |
| | PHUC T. DANG | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *January 9, 2004*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *15 November 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 010904
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

PHUC T. DANG PD
PRIMARY EXAMINER

## DETAILED ACTION

### Examiner's Statement of Reasons for Allowance

1. Claims 1-20 are allowed.

2. The following is an examiner's statement of reasons for allowance:

None of the prior art teaches a method for fabricating a gate structure for a semiconductor device, the gate structure being formed on a substrate, the gate being adjacent to a dielectric material having a top surface, the method comprising the step of removing a first potion of the silicon layer and a first portion of the inner spacer layer, so that the top surface of the dielectric material is exposed and a second portion of the silicon layer and a second portion of the inner spacer layer remain in the gate region and have surfaces coplanar with the top surface in combination with the other steps found in the independent method claims 1.

None of the prior art teaches a method for fabricating a gate structure for a semiconductor device, the gate structure being formed on a substrate, the gate being adjacent to a dielectric material having a top surface, the method comprising the step of removing a first potion of the silicon layer, so that the top surface of the dielectric material is exposed and a second portion of the silicon layer remains in the gate region and has a surface coplanar with the top surface in combination with the other steps found in the independent method claims 8.

None of the prior art teaches a semiconductor device having a gate structure on a substrate, the gate structure being adjacent to a dielectric material having a top surface, the device comprising a silicide structure having an upper surface coplanar with the top surface,

Wherein the gate region is characterized as a trench having a bottom and sidewalls, the gate dielectric overlies the bottom of the trench, the inner spacer layer is in contact with the sidewalls of the trench, and the silicide structure fills the trench in combination with the other structure in the apparatus independent claim 15.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

4. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and for After Final communications.

5. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang PD

Primary Examiner

Art Unit 2818